library ieee;

use ieee.std\_logic\_1164.all;

entity AdderTB is

end AdderTB;

architecture Testbench of AdderTB is

component adder is

port(a,b,cin: in std\_logic;

sum,cout: out std\_logic);

end component;

signal a,b,cin,sum,cout: std\_logic;

begin

ust: adder port map(a,b,cin,sum,cout);

process

begin

a<='0';

b<='0';

cin<='0';

wait for 50 ns;

a<='1';

b<='0';

cin<='0';

wait for 50 ns;

a<='0';

b<='1';

cin<='0';

wait for 50 ns;

a<='1';

b<='1';

cin<='0';

wait for 50 ns;

a<='0';

b<='0';

cin<='1';

wait for 50 ns;

a<='1';

b<='0';

cin<='1';

wait for 50 ns;

a<='0';

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cin<='1';

wait for 50 ns;

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b<='1';

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end process;

end Testbench;

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end process;

end Testbench;